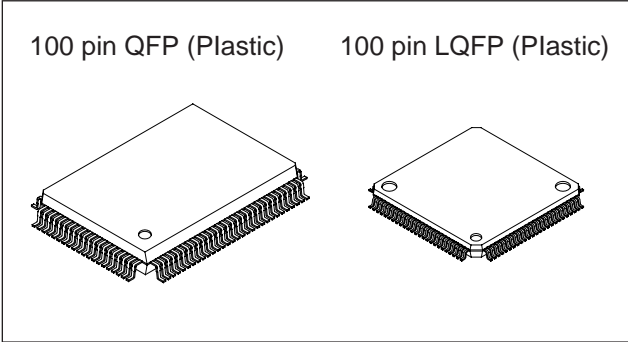


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP87132/87140 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface (2ch independently), timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit (PPG 2ch independently, RTG 2ch independently), PWM generator, general purpose prescaler, PWM for tuner, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP87132/87140 provides power on reset function, sleep/stop function which enables to lower power consumption.



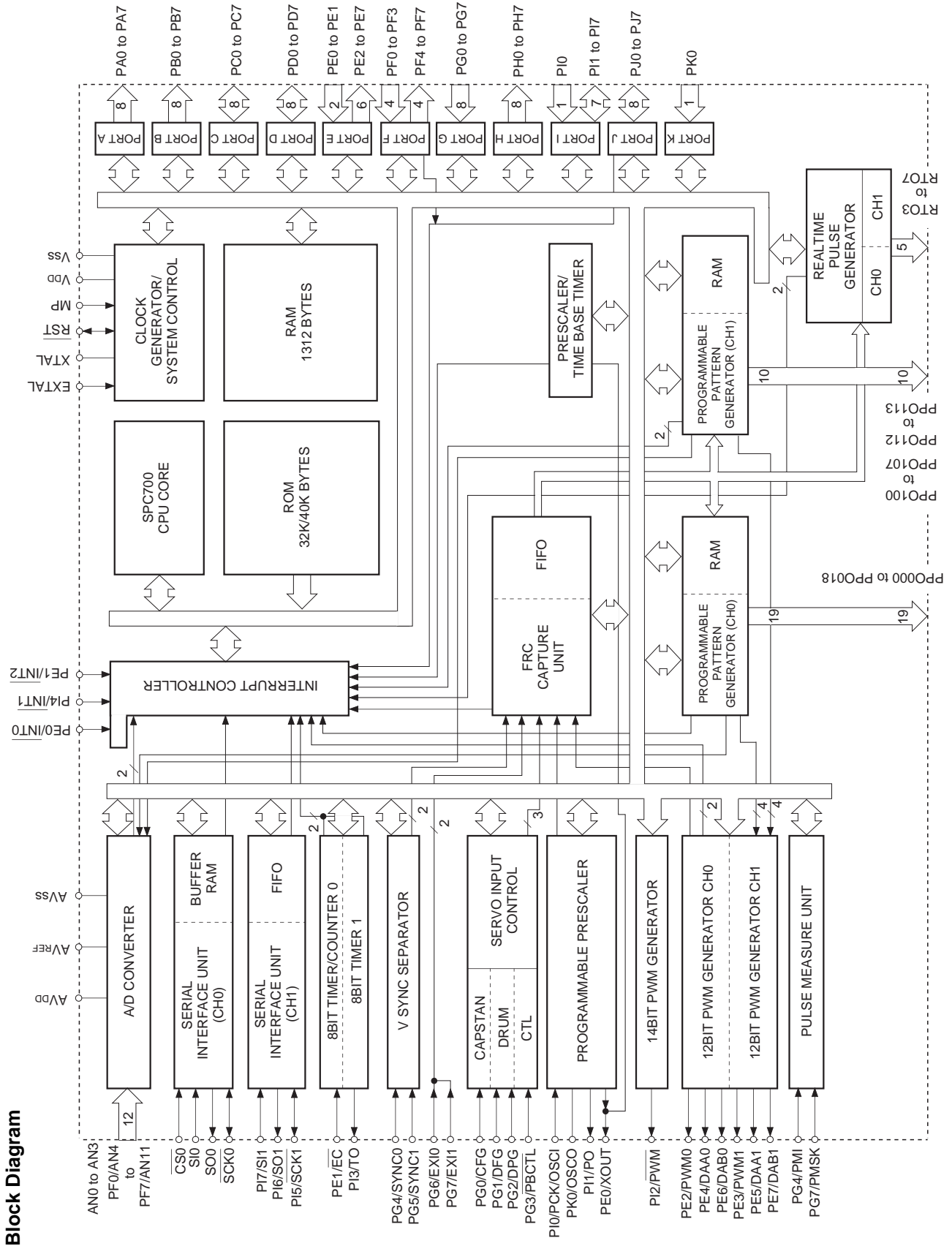
**Structure**

Silicon gate CMOS IC

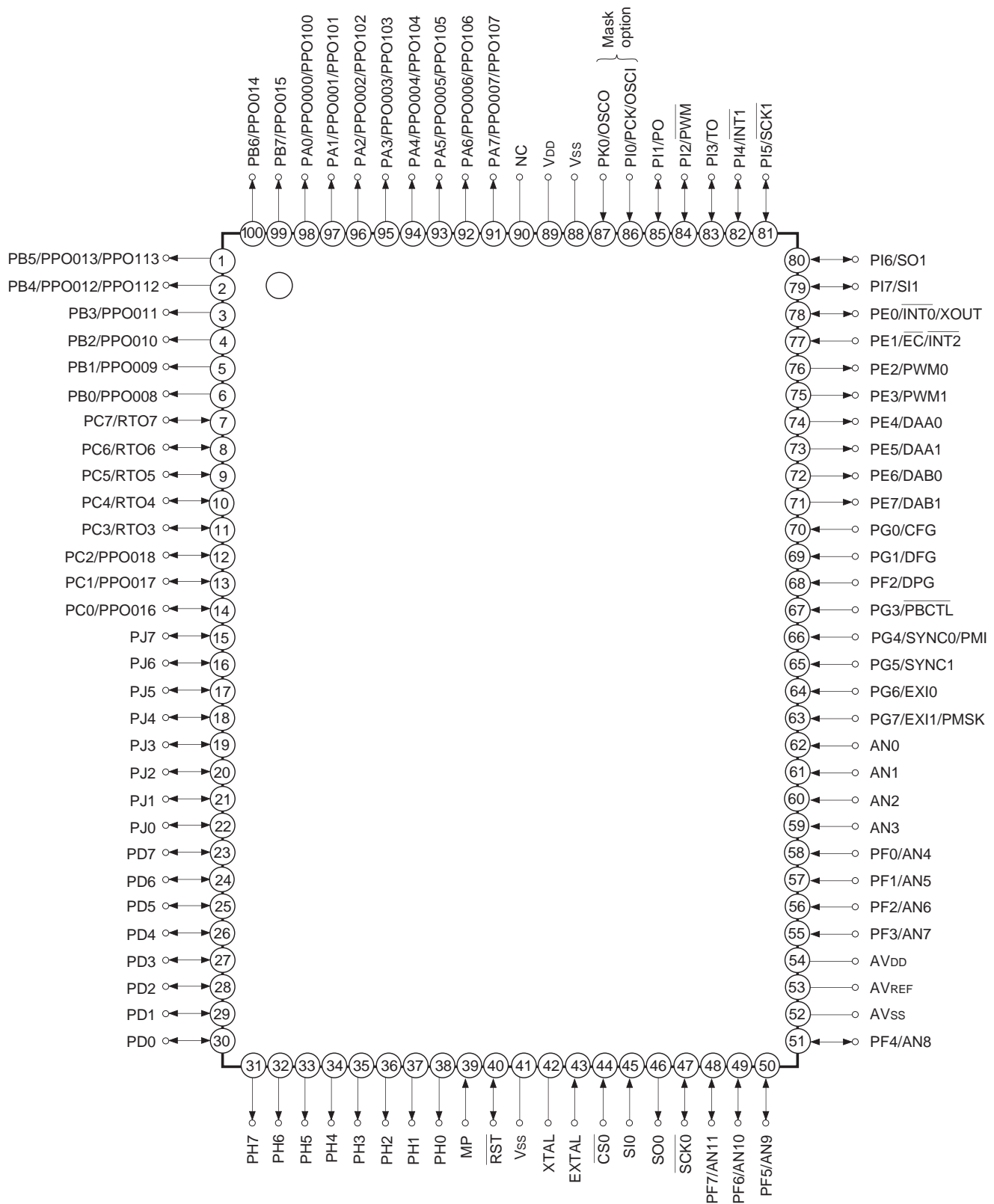
**Features**

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
  - During operation 333ns/12MHz (3.0 to 5.5V)
  - During operation 250ns/16MHz (4.5 to 5.5V)
- Incorporated ROM capacity
  - 32K bytes (CXP87132)
  - 40K bytes (CXP87140)
- Incorporated RAM capacity
  - 1312 bytes
- Peripheral functions
  - A/D converter
    - 8-bit, 12-channel, successive approximation system (Conversion time: 20µs/16MHz)
  - Serial I/O
    - Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel
    - Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer) 1-channel
  - Timer
    - 8-bit timer, 8-bit timer/counter, 19-bit time base timer
  - High precision timing pattern generator
    - PPG 19 pins 32-stage programmable
    - PPG 10 pins 21-stage programmable
    - RTG 5 pins 2-channel
  - PWM/DA gate output
    - PWM 12-bit, 2-channel (Repetitive frequency 62.5kHz/16MHz)
    - DA gate pulse 12-bit, 4-channel
  - Servo input control
    - Capstan FG, Drum FG/PG, CTL input
  - VSYNC separator
    - Incorporated 26-bit and 8-stage FIFO
  - FRC capture unit
    - 14-bit, 1-channel
  - PWM output
    - 10-bit (System clock asynchronous)
  - General purpose prescaler
  - Pulse cycle measuring circuit
- Interruption
  - 18 factors, 14 vectors, multi-interruption possible
- Standby mode
  - Sleep/stop
- Package
  - 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip
  - CXP87100 100-pin ceramic QFP/LQFP

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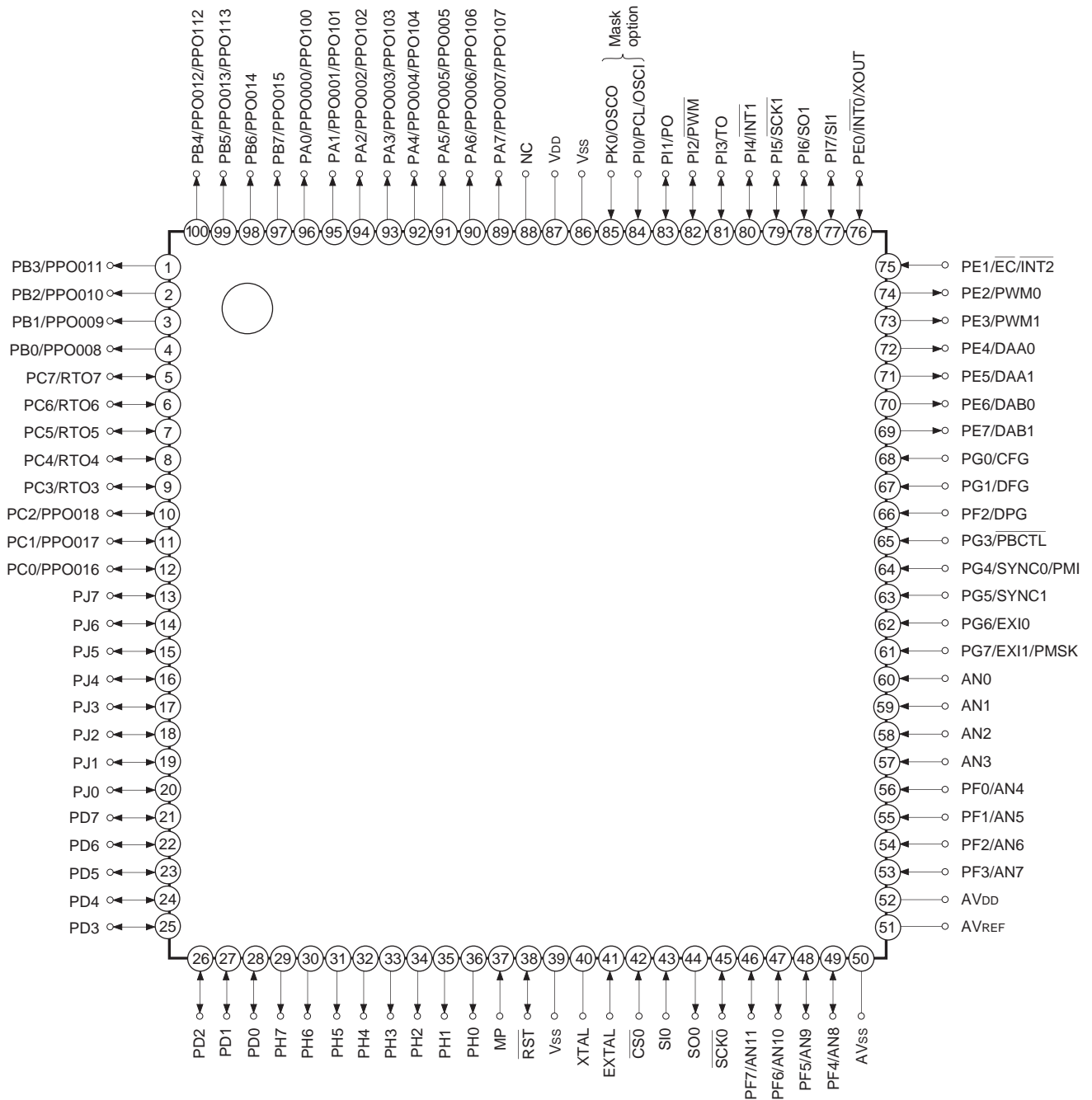


Pin Configuration 1 (Top View) 100 pin QFP Package



- Note)**
1. NC (Pin 90) is always connected to V<sub>DD</sub>.
  2. V<sub>SS</sub> (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP Package



- Note)**
1. NC (Pin 88) is always connected to V<sub>DD</sub>.
  2. V<sub>SS</sub> (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG0, PPG1) output. Functions as high precision real time pulse output port. ( PPG0 19 pins ) ( PPG1 10 pins )	
PB0/PPO008 to PB7/PPO015	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)		
PC0/PPO016 to PC2/PPO018	I/O/ Real time output	(Port C) 8-bit I/O port. Enables to specify I/O by a bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (During 5V ± 0.5V operation) (8 pins)		
PE0/ $\overline{\text{INT0}}$ /XOUT	Input/Input/Output	(Port E) 8-bit port. Lower 2 bits are input port and upper 6 bits are output port. (8 pins)	Input pin to request external interruption. Active when falling edge.	1/2 dividing clock output of XTAL or OSCO.
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output		DA gate pulse output pins. (4 pins)	
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Output	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

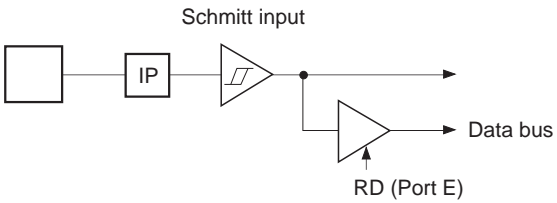
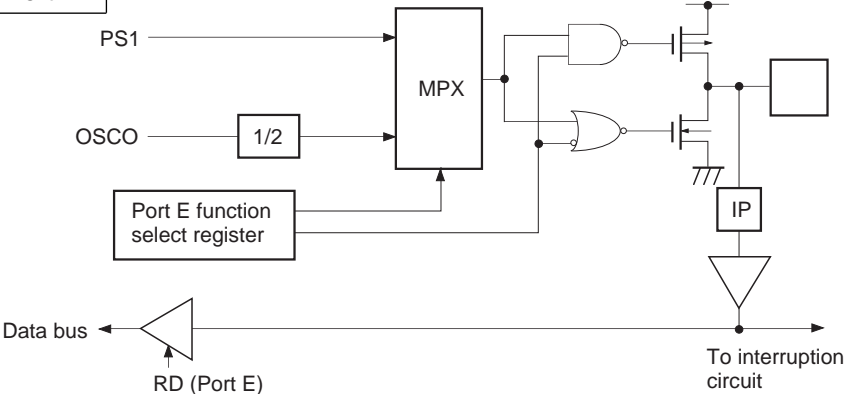
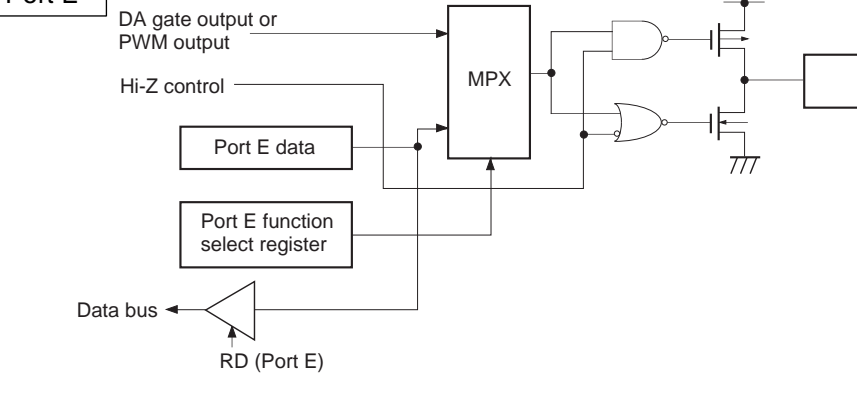
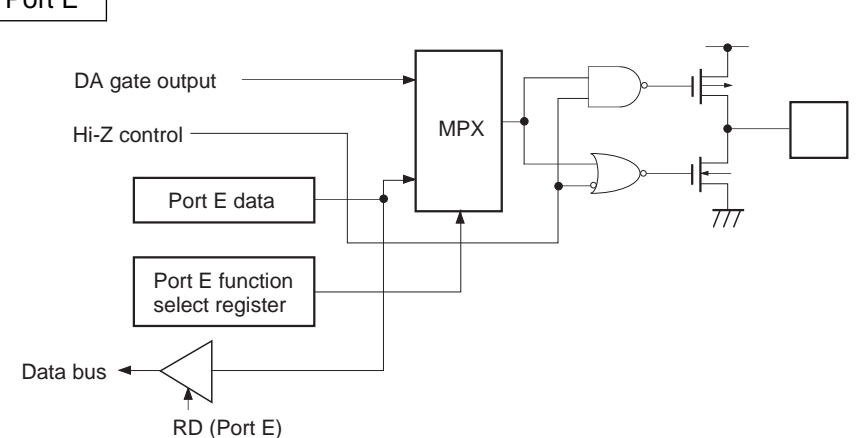
Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/PBCTL	Input/Input		Playback CTL pulse input pin.	
PG4/SYNC0 /PMI	Input/Input/Input		Composite sync signal input pin.	Measuring pulse signal input pin of pulse cycle measuring unit.
PG5/SYNC1	Input/Input			
PG6/EXI0	Input/Input		External input pin to FRC capture unit.	
PG7/EXI1/ PMSK	Input/Input/Input			Measuring enable signal input pin of pulse cycle measuring unit.
PH0 to PH7	Output	(Port H) 8-bit output port; large current, N-ch open drain output. (8 pins)		
PI0/PCK /OSCI	Input/Input/Input	(Port I) Lower 1 bit is input port (mask option) and upper 7 bits are I/O port. I/O port can be specified by a bit unit. (8 pins)	External clock input pin of general purpose prescaler.	Connecting pin of crystal for general purpose prescaler oscillation circuit. (Mask option)
PI1/PO	I/O/Output		General purpose prescaler output pin.	
PI2/PWM	I/O/Output		14-bit PWM output pin.	
PI3/TO	I/O/Output		Timer/counter output pin. (duty = 50%)	
PI4/INT1	I/O/Input		Input pin to request external interruption. Active when falling edge.	
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.	
PI6/SO1	I/O/Output		Serial data (CH1) output pin.	
PI7/SI1	I/O/Input		Serial data (CH1) input pin.	
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by a bit unit. I/O can be specified by a bit unit.		

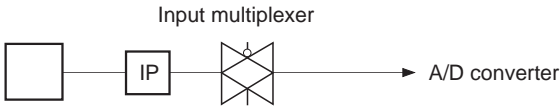
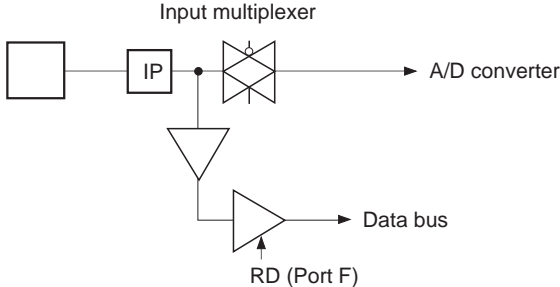
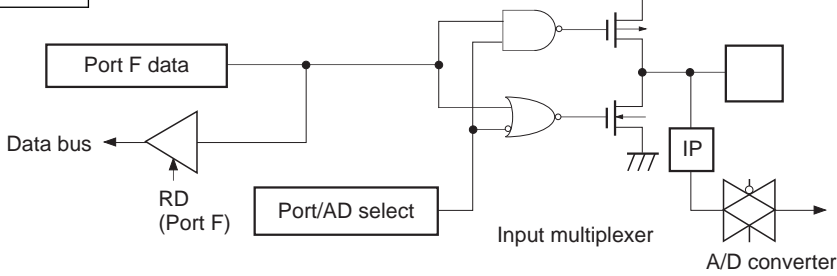
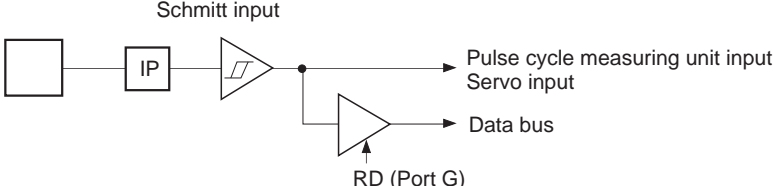
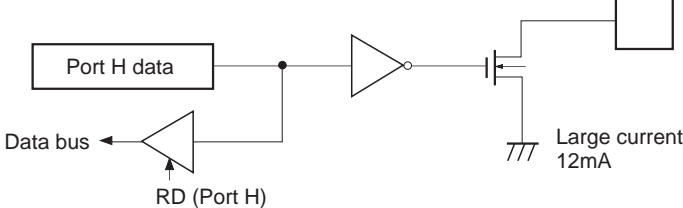
Symbol	I/O	Description	
PK0/OSCO	Input/Output	Input port. (Mask option)	Connecting pin of crystal for general purpose prescaler oscillation circuit. (Mask option)
EXTAL	Input	Connecting pin of crystal for system clock oscillation. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	System reset pin of active "L" level. $\overline{\text{RST}}$ pin is I/O pin, which outputs "L" level by incorporated power on reset function when power on. (Mask option)	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVSS		GND pin of A/D converter.	
VDD		Positive power supply pin.	
VSS		GND pin. Connect both Vss pins to GND.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107 PB4/PPO012 /PPO112 to PB5/PPO013 /PPO113 10 pins	<p>Port A Port B</p> <p>Output becomes active from high impedance by data writing to port register.</p>	Hi-Z
PB0/PPO008 to PB3/PPO011 PB6/PPO014 to PB7/PPO015 6 pins	<p>Port B</p> <p>Output becomes active from high impedance by data writing to port register.</p>	Hi-Z
PC0/PPO016 to PC2/PPO018 PC3/RTO3 to PC7/RTO7 8 pins	<p>Port C</p> <p>(Every bit)</p> <p>Input protection circuit</p>	Hi-Z
PD0 to PD7 8 pins	<p>Port D</p> <p>(Every 4 bits) (PD0 to PD3) (PD4 to PD7)</p> <p>Large current 12mA</p>	Hi-Z



Pin	Circuit format	When reset
<p>PE1/<math>\overline{\text{EC}}/\overline{\text{INT2}}</math></p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}/\text{XOUT}</math></p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>High level</p>

Pin	Circuit format	When reset
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	<p>Port F</p> 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	<p>Port F</p> 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0/PMI PG5/SYNC1 PG6/EXI0 PG7/EXI1/PMSK 8 pins	<p>Port G</p>  <p>Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.</p>	Hi-Z
PH0 to PH7 8 pins	<p>Port H</p> 	Hi-Z

Pin	Circuit format	When reset
<p>PI1/PO PI2/PWM PI3/TO</p> <p>3 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>(PI1: From general purpose prescaler PI2: From 14-bit PWM PI3: From timer/counter)</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI4/<math>\overline{\text{INT1}}</math> PI7/SI1</p> <p>2 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>Schmitt input</p> <p>PI4: To interruption circuit PI7: To serial CH1</p>	<p>Hi-Z</p>
<p>PI5/<math>\overline{\text{SCK1}}</math> PI6/SO1</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>Note) PI5 is schmitt input PI6 is inverter input</p> <p>To serial CH1</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p> <p>Port J data</p> <p>Port J direction</p> <p>Data bus</p> <p>RD (Port J)</p> <p>IP</p> <p>Edge detection</p> <p>Standby release</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
CS0 SIO 2 pins	<p>Schmitt input</p>	Hi-Z
SO0 1 pin		Hi-Z
SCK0 1 pin		Hi-Z
EXTAL XTAL 2 pins	<ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	Oscillation
RST 1 pin		Low level
MP 1 pin		Hi-Z
PI0/PCK/OSCI PK0/OSCO 2 pins	<div style="display: flex; flex-direction: column;"> <div style="margin-bottom: 10px;"> <p>Port I Port K</p> <p style="text-align: center;"><b>Fig. 1</b></p> </div> <div> <p style="text-align: center;"><b>Fig. 2</b></p> </div> </div> <p>Note) Circuit format of Fig. 1 or Fig. 2 can be selected with mask option.</p>	<p>Oscillation</p> <p>Hi-Z</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of output pins
Low level output current	I <sub>OL</sub>	15	mA	Other than large current output pins
	I <sub>OLC</sub>	20	mA	Large current output pin* <sup>3</sup>
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP
		380		LQFP

\*<sup>1</sup> AV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*<sup>2</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V. ( $\overline{CS0}$ ,  $\overline{SI0}$ , PG and PH excluded.)

\*<sup>3</sup> The large current operation transistors are the N-CH transistors of the PD and PH ports.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5	V	Guaranteed data hold operation range during stop
Analog power supply	AV <sub>DD</sub>	3.0	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pins
			5.5	V	CMOS schmitt input*4
	V <sub>IHTS</sub>	2.2	5.5	V	TTL schmitt input*5, *8
V <sub>IHEX</sub>	V <sub>DD</sub> + 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*6	
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2, *8
			0.2V <sub>DD</sub>	V	*2, *7
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS schmitt input*3, *4 and PE0/ $\overline{\text{INT0}}$ pins
	V <sub>ILTS</sub>	0	0.8	V	TTL schmitt input*5, *8
V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*6	
Operating temperature	Topr	-20	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*2 Normal input port (each pin of PC, PD, PF0 to PF3, PI, PJ, and PK), MP pin.

\*3 Each pin of  $\overline{\text{SCK0}}$ ,  $\overline{\text{RST}}$ , PE1/ $\overline{\text{EC/INT2}}$ , PI1/ $\overline{\text{PO}}$ , PI4/ $\overline{\text{INT1}}$ , PI5/ $\overline{\text{SCK1}}$  and PI7/ $\overline{\text{SI1}}$ .

\*4 Each pin of  $\overline{\text{CS0}}$ , SI0, and PG (for PG4 and PG5, when CMOS schmitt input is selected.)

\*5 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

\*6 It specifies only when the external clock is input.

\*7 In case of 3.0 to 3.6V supply voltage (V<sub>DD</sub>).

\*8 In case of 4.5 to 5.5V supply voltage (V<sub>DD</sub>).

**Electrical Characteristics**

**DC Characteristics**

Supply voltage (V<sub>DD</sub>) 4.5 to 5.5V

(T<sub>a</sub> = -20 to +75°C, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PE, PF4 to PF7, PH (V <sub>OL</sub> only)	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
Low level output voltage	V <sub>OL</sub>	PI1 to PI7, PJ, SO, SCK, RST* <sup>1</sup> (V <sub>OL</sub> only)	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA			0.6	V
		PD, PH	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA			1.5	V
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
	I <sub>ILE</sub>		V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.5		-40	μA
	I <sub>ILR</sub>	RST* <sup>2</sup>	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5		-400	μA
I/O leakage current	I <sub>Iz</sub>	PA to PK, MP, AN0 to AN3, CS, SI, SO, SCK, RST* <sup>2</sup>	V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0, 5.5V			±10	μA
Supply current* <sup>3</sup>	I <sub>DD1</sub>	V <sub>DD</sub>	Crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF) of 16MHz		25	45	mA
	I <sub>DDS1</sub>		V <sub>DD</sub> = 5V ± 10%* <sup>4</sup>				
			Sleep mode		1	5	mA
I <sub>DDS3</sub>	Stop mode	V <sub>DD</sub> = 5V ± 10%					
		V <sub>DD</sub> = 5.5V			10	μA	
Input capacity	C <sub>IN</sub>	Other than V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , and AV <sub>SS</sub> pins	Clock 1MHz 0V for no measured pins		10	20	pF

\*1 RST pin specifies only when the power on reset circuit has been selected with mask option.

\*2 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistance is selected.

\*3 When entire output pins are open.

\*4 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

Supply voltage (V<sub>DD</sub>) 3.0 to 3.6V

(T<sub>a</sub> = -20 to +75°C, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PE, PF4 to PF7, PH (V <sub>OL</sub> only)	V <sub>DD</sub> = 3.0V, I <sub>OH</sub> = -0.15mA	2.7			V
			V <sub>DD</sub> = 3.0V, I <sub>OH</sub> = -0.5mA	2.3			V
Low level output voltage	V <sub>OL</sub>	PI1 to PI7, PJ, SO, SCK, RST*1 (V <sub>OL</sub> only)	V <sub>DD</sub> = 3.0V, I <sub>OL</sub> = 1.2mA			0.3	V
			V <sub>DD</sub> = 3.0V, I <sub>OL</sub> = 1.6mA			0.5	V
			PD, PH	V <sub>DD</sub> = 3.0V, I <sub>OL</sub> = 5.0mA			1.0
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 3.6V, V <sub>IH</sub> = 3.6V	0.3		20	μA
	I <sub>IIE</sub>		V <sub>DD</sub> = 3.6V, V <sub>IL</sub> = 0.3V	-0.3		-20	μA
	I <sub>ILR</sub>	RST*2	V <sub>DD</sub> = 3.6V, V <sub>IL</sub> = 0.3V	-0.9		-200	μA
I/O leakage current	I <sub>Iz</sub>	PA to PK, MP, AN0 to AN3, CS, SI, SO, SCK, RST*2	V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0, 5.5V			±10	μA
Supply current*3	I <sub>DD2</sub>	V <sub>DD</sub>	Crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF) of 12MHz		12	25	mA
	I <sub>DDS2</sub>		V <sub>DD</sub> = 3.3V ± 0.3V*4				
			Sleep mode		0.5	2.5	mA
I <sub>DDS3</sub>	Stop mode						
	V <sub>DD</sub> = 5.5V				10	μA	
Input capacity	C <sub>IN</sub>	Other than V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , and AV <sub>SS</sub> pins	Clock 1MHz 0V for no measured pins		10	20	pF

\*1 RST pin specifies only when the power on reset circuit has been selected with mask option.

\*2 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistance is selected.

\*3 When entire output pins are open.

\*4 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE<sub>H</sub>) to "00" and operating in high speed mode (1/2 dividing clock).



AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	VDD = 4.5 to 5.5V	28		ns
					37.5		
System clock input rising and falling times	t <sub>CR</sub> , t <sub>CF</sub>	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns	
Event count clock input pulse width	t <sub>EL</sub> , t <sub>EH</sub>	PE1/ $\overline{EC}$	Fig. 3		t <sub>sys</sub> × 4*1	ns	
Event count clock input rising and falling times	t <sub>ER</sub> , t <sub>EF</sub>	PE1/ $\overline{EC}$	Fig. 3		20	ms	

\*1 t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

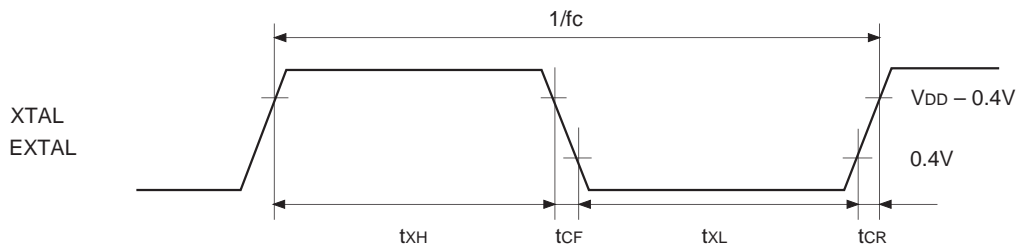


Fig. 1. Clock timing

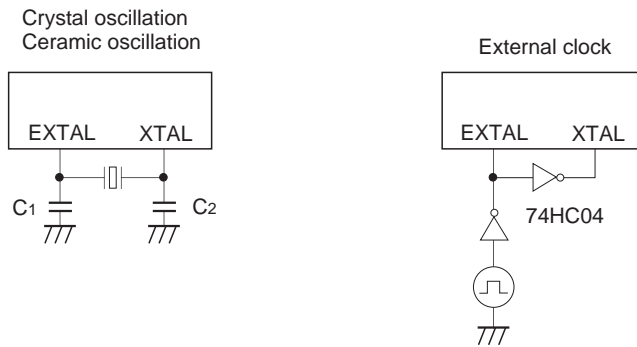


Fig. 2. Clock applied condition

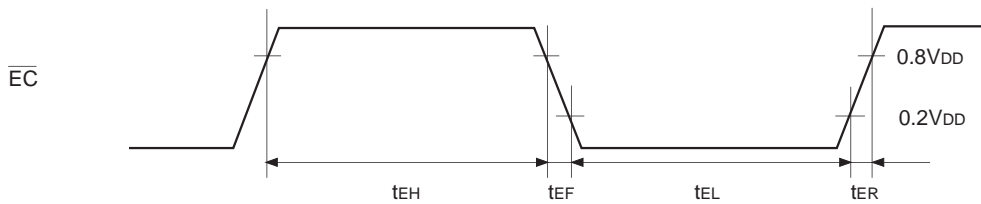


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	$t_{DCSK}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK0}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	$t_{DCSKF}$	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK0}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	$t_{DCSO}$	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	$t_{DCSOF}$	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS}$ High level width	$t_{WHCS}$	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK}$ cycle time	$t_{KCY}$	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{SCK}$ High and Low level widths	$t_{KH}$ $t_{KL}$	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 100$		ns
SI input setup time (against $\overline{SCK} \uparrow$ )	$t_{SIK}$	SI0	$\overline{SCK}$ input mode	$-t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$ )	$t_{KSI}$	SI0	$\overline{SCK}$ input mode	$2t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	$t_{KSO}$	SO0	$\overline{SCK}$ input mode		$2t_{sys} + 200$	ns
			$\overline{SCK}$ output mode		100	ns

**Note 1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys}$  [ns] = 2000/ $f_c$  (Upper 2 bits = "00"), 4000/ $f_c$  (Upper 2 bits = "01"), 16000/ $f_c$  (Upper 2 bits = "11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO means each pin of  $\overline{CS} \rightarrow \overline{CS0}$ ,  $\overline{SCK} \rightarrow \overline{SCK0}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF + 1TTL.

**Serial transfer (CH0)**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $3.6\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	$t_{\text{DCSK}}$	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 250$	ns
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ floating delay time	$t_{\text{DCSKF}}$	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{DCSO}}$	SO0	Chip select transfer mode		$t_{\text{sys}} + 250$	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ floating delay time	$t_{\text{DCSOF}}$	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}}$ High level width	$t_{\text{WHCS}}$	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ High and Low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 150$		ns
SI input setup time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI0	$\overline{\text{SCK}}$ input mode	$-t_{\text{sys}} + 100$		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI0	$\overline{\text{SCK}}$ input mode	$2t_{\text{sys}} + 100$		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO0	$\overline{\text{SCK}}$ input mode		$2t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK}}$ output mode		125	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns] =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

**Note 2)**  $\overline{\text{CS}}$ ,  $\overline{\text{SCK}}$ , SI and SO means each pin of  $\overline{\text{CS}} \rightarrow \overline{\text{CS0}}$ ,  $\overline{\text{SCK}} \rightarrow \overline{\text{SCK0}}$ , SI  $\rightarrow$  SI0, and SO  $\rightarrow$  SO0 respectively.

**Note 3)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF.

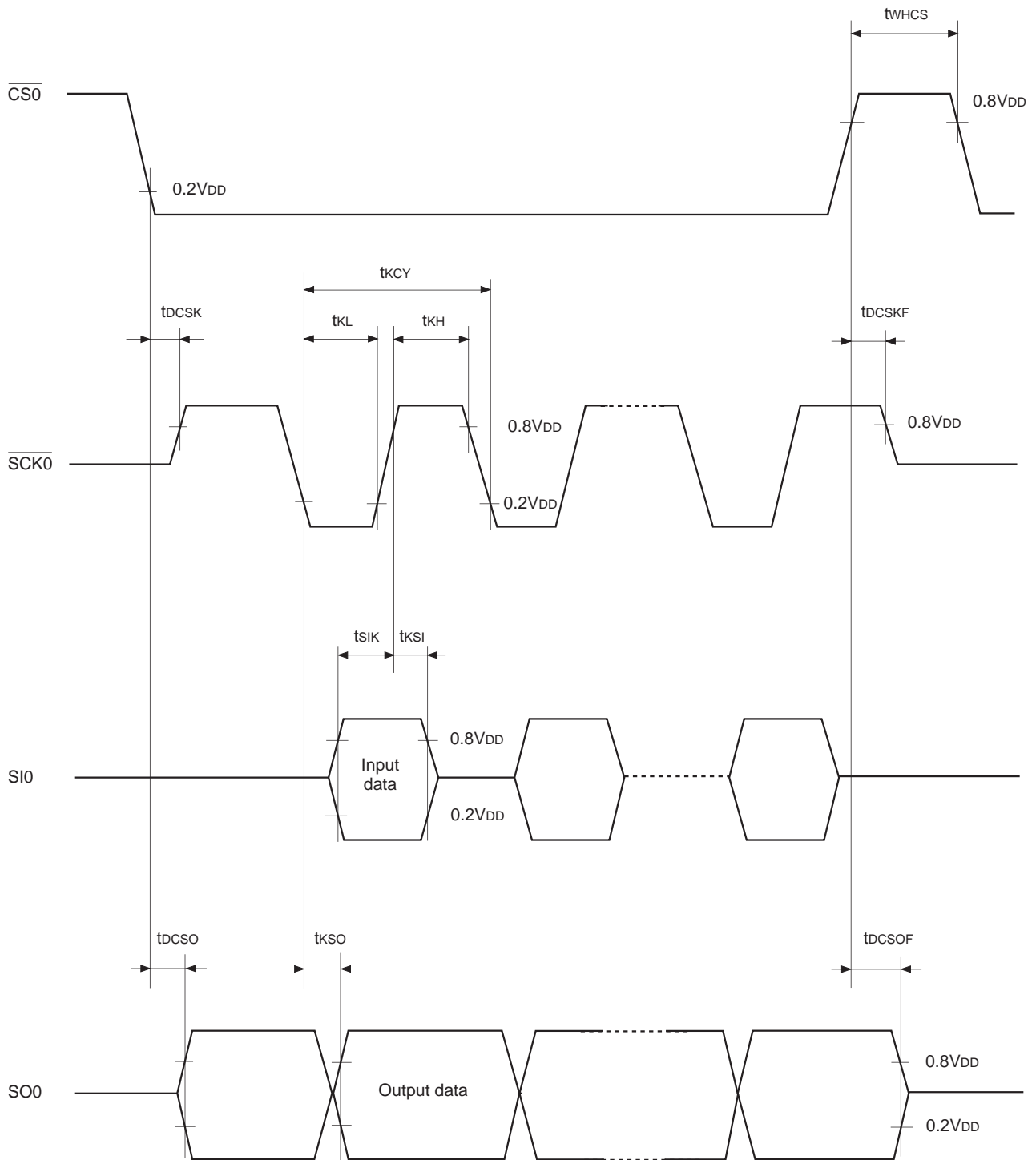


Fig. 4. Serial transfer timing (CH0)

**Serial transfer (CH1) (SIO mode)**

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t <sub>KCY</sub>	$\overline{\text{SCK1}}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
SCK1 High and Low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{\text{SCK1}}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 50		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t <sub>SIK</sub>	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t <sub>KSI</sub>	SI1	$\overline{\text{SCK1}}$ input mode	t <sub>sys</sub> + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t <sub>KSO</sub>	SO1	$\overline{\text{SCK1}}$ input mode		t <sub>sys</sub> + 200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF + 1TTL.

**Serial transfer (CH1) (SIO mode)**

(Ta = -20 to +75°C, V<sub>DD</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t <sub>KCY</sub>	$\overline{\text{SCK1}}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
SCK1 High and Low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{\text{SCK1}}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 150		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t <sub>SIK</sub>	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t <sub>KSI</sub>	SI1	$\overline{\text{SCK1}}$ input mode	t <sub>sys</sub> + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t <sub>KSO</sub>	SO1	$\overline{\text{SCK1}}$ input mode		t <sub>sys</sub> + 250	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF.

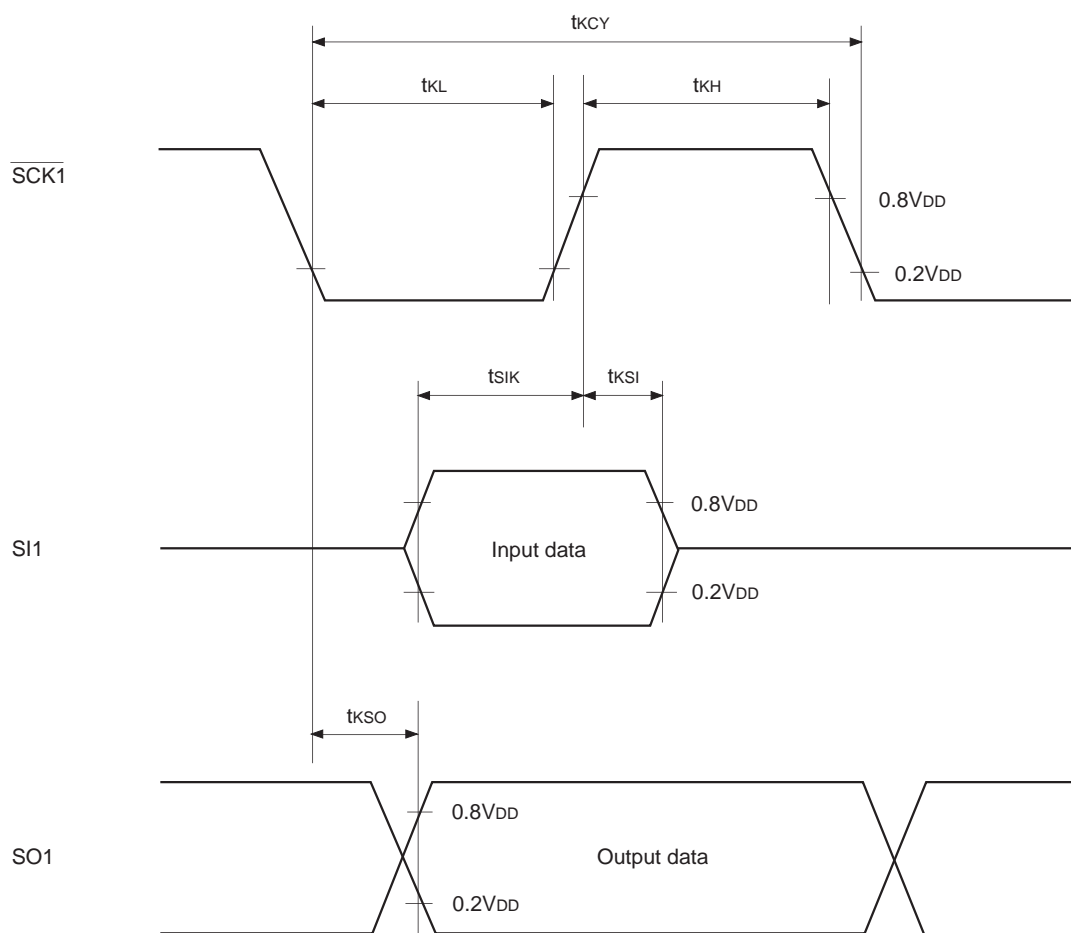


Fig. 5. Serial transfer CH1 timing (SIO mode)

**Serial transfer (CH1) (Special mode)** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	<b>Note 1)</b>		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

**Note 1)**  $t_{LCY}$  specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at  $104\mu\text{s}$ .

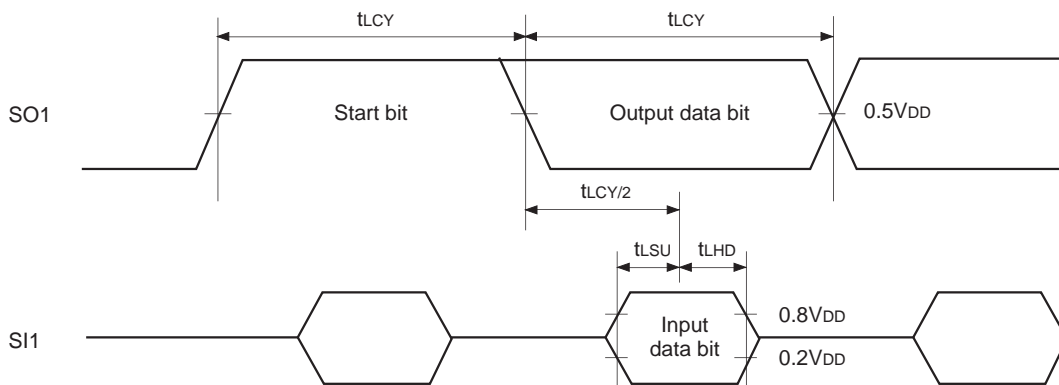
**Note 2)** The load of SO1 pin is  $50\text{pF} + 1\text{TTL}$ .

**Serial transfer (CH1) (Special mode)** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $3.6\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	<b>Note 1)</b>		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

**Note 1)**  $t_{LCY}$  specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at  $104\mu\text{s}$ .

**Note 2)** The load of SO1 pin is  $50\text{pF}$ .



**Fig. 6. Serial transfer CH1 timing (Special mode)**

**(3) A/D converter characteristics**

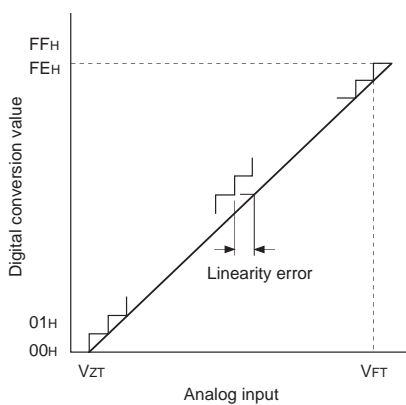
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 1$	LSB
Absolute error						$\pm 2$	LSB
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*1}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*1}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$	$V_{DD} = AV_{DD} = 4.5$ to $5.5\text{V}$	$AV_{DD} - 0.5$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	$AN0$ to $AN11$		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operating mode $AV_{REF} = 4.0$ to $5.5\text{V}$		0.6	1.0	mA
			Sleep mode Stop mode			10	$\mu\text{A}$

**A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 3.0$  to  $3.6\text{V}$ ,  $AV_{REF} = 2.7$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 3.3\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 1$	LSB
Absolute error						$\pm 2$	LSB
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*1}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*1}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$	$V_{DD} = AV_{DD} = 3.0$ to $3.6\text{V}$	$AV_{DD} - 0.3$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	$AN0$ to $AN11$		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operating mode $AV_{REF} = 2.7$ to $3.6\text{V}$		0.4	0.7	mA
			Sleep mode Stop mode			10	$\mu\text{A}$



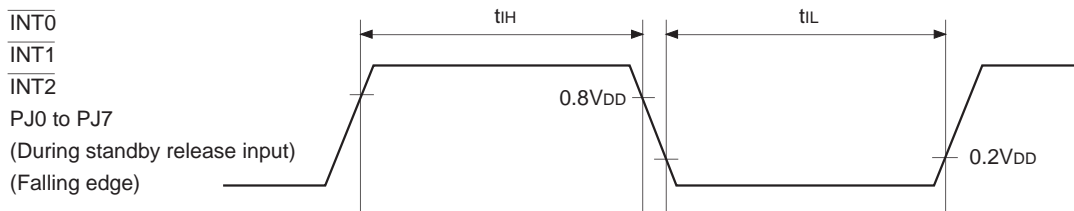
\*1 The value of  $f_{ADC}$  is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).  
 When PS2 is selected,  $f_{ADC} = f_c/2$   
 When PS1 is selected,  $f_{ADC} = f_c$

**Fig. 7. Definitions of A/D converter terms**

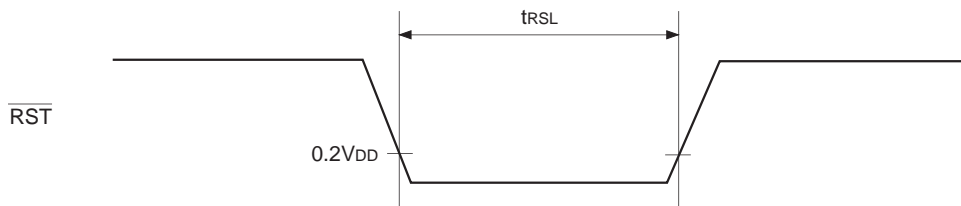


**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ PJ0 to PJ7		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs



**Fig. 8. Interruption input timing**



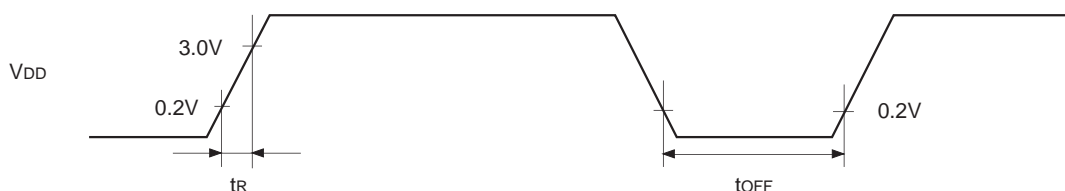
**Fig. 9. Reset input timing**

**(5) Power on reset**

Power on reset\* (Ta = -20 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising edge	t <sub>R</sub>	VDD	Power on reset	0.05	30	ms
Power supply cut-off time	t <sub>OFF</sub>		Repetitive power on reset	1		ms

\* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

**Fig. 10. Power on reset**

**(6) General purpose prescaler**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	$f_{PCK}$	PCK				12	MHz
External clock input pulse width	$t_{WH}, t_{WL}$	PCK		33			ns
External clock input rising and falling times	$t_R, t_F$	PCK				200	ns
Prescaler output delay time (against PCK $\uparrow$ )	$t_{PLH}$	PO	External clock input PCK $t_R = t_F = 6\text{ns}$		80	130	ns
	$t_{PHL}$				60	100	ns
Prescaler output rising and falling times	$t_{TLH}$	PO	External clock input PCK $t_R = t_F = 6\text{ns}$		50	100	ns
	$t_{TLH}$				20	40	ns

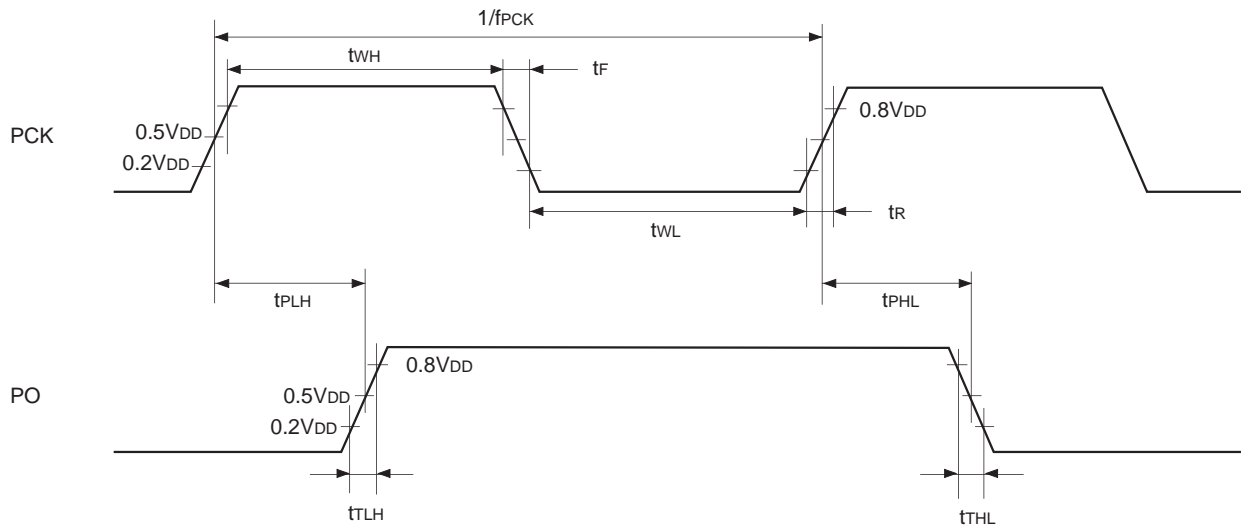
**Note)** The load of PO pin is 50pF.

**General purpose prescaler**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $3.6\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	$f_{PCK}$	PCK				12	MHz
External clock input pulse width	$t_{WH}, t_{WL}$	PCK		33			ns
External clock input rising and falling times	$t_R, t_F$	PCK				200	ns
Prescaler output delay time (against PCK $\uparrow$ )	$t_{PLH}$	PO	External clock input PCK $t_R = t_F = 6\text{ns}$		130	220	ns
	$t_{PHL}$				90	150	ns
Prescaler output rising and falling times	$t_{TLH}$	PO	External clock input PCK $t_R = t_F = 6\text{ns}$		100	280	ns
	$t_{TLH}$				30	70	ns

**Note)** The load of PO pin is 50pF.



**Fig. 11. General purpose prescaler timing**

## (7) Others

(Ta = -20 to +75°C, V<sub>DD</sub> = 3.0 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t <sub>CFH</sub> t <sub>CFL</sub>	CFG		t <sub>FRC</sub> × 24 + 200		ns
DFG input high and low level widths	t <sub>DFH</sub> t <sub>DFL</sub>	DFG		t <sub>FRC</sub> × 8 + 200		ns
DPG minimum pulse width	t <sub>DPW</sub>	DPG		50		ns
DPG minimum removal time	t <sub>rem</sub>	DPG		50		ns
PBCTL input high and low level widths	t <sub>CTH</sub> t <sub>CTL</sub>	PBCTL	t <sub>sys</sub> = 2000/fc	t <sub>FRC</sub> × 8 + t <sub>sys</sub> + 200		ns
EXI input high and low level widths	t <sub>EIH</sub> t <sub>EIL</sub>	EXI0 EXI1	t <sub>sys</sub> = 2000/fc	t <sub>FRC</sub> × 8 + t <sub>sys</sub> + 200		ns
PMI input high and low level widths	t <sub>PIH</sub> t <sub>PIL</sub>	PMI		t <sub>sys</sub> + 200		ns
PMSK input high and low level widths	t <sub>PSH</sub> t <sub>PSL</sub>	PMSK		t <sub>sys</sub> + 200		ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** The value of t<sub>FRC</sub> is as follows by selecting FRC clock (FRCS: 01EEH bit 7)

When PS0 is selected, t<sub>FRC</sub> = 1000/fc (ns)

When PS1 is selected, t<sub>FRC</sub> = 2000/fc (ns)

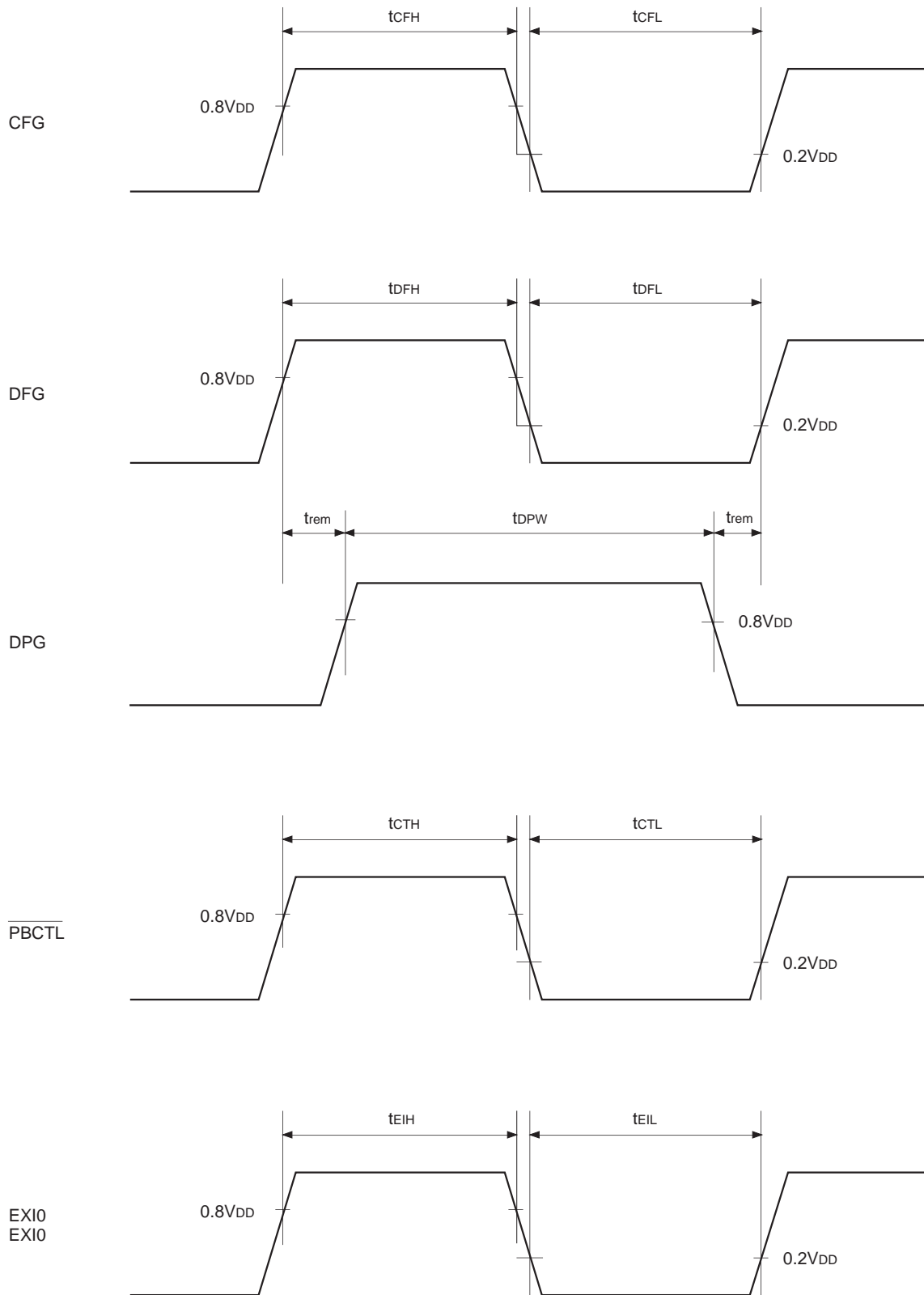
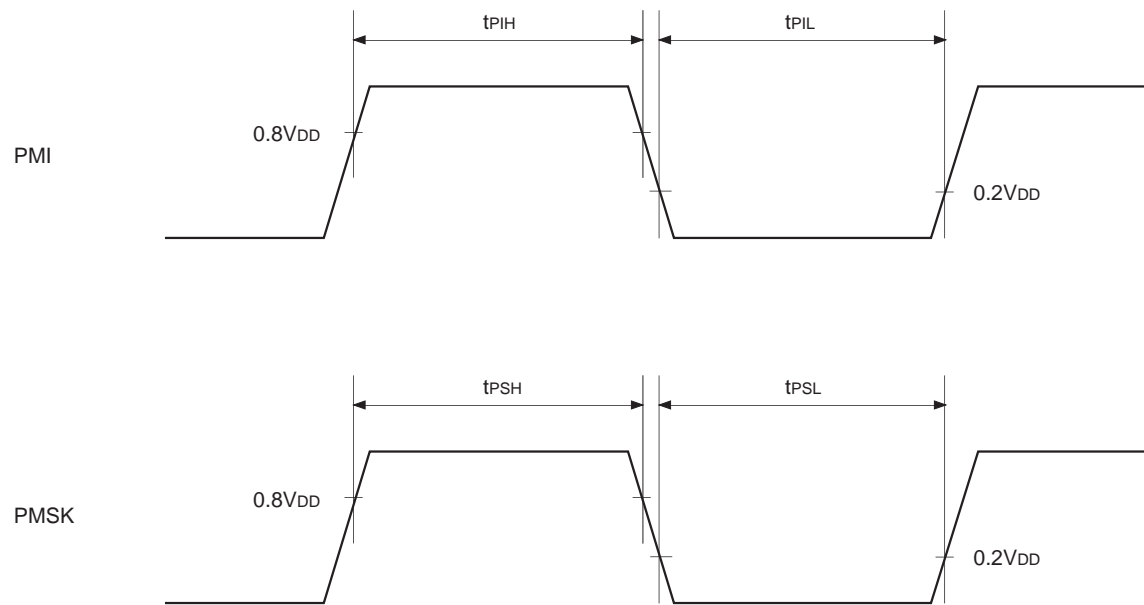


Fig. 12. Other timings



Supplement

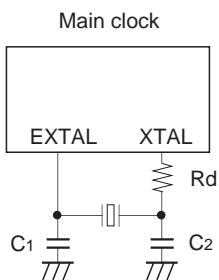


Fig. 13. Recommended oscillation circuit

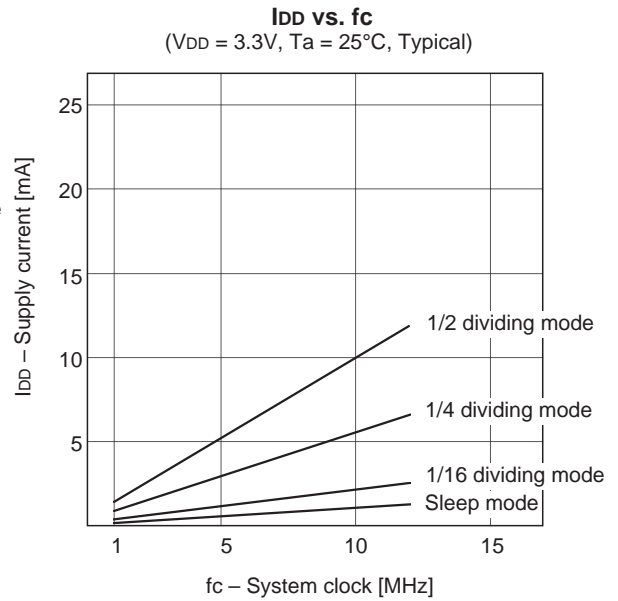
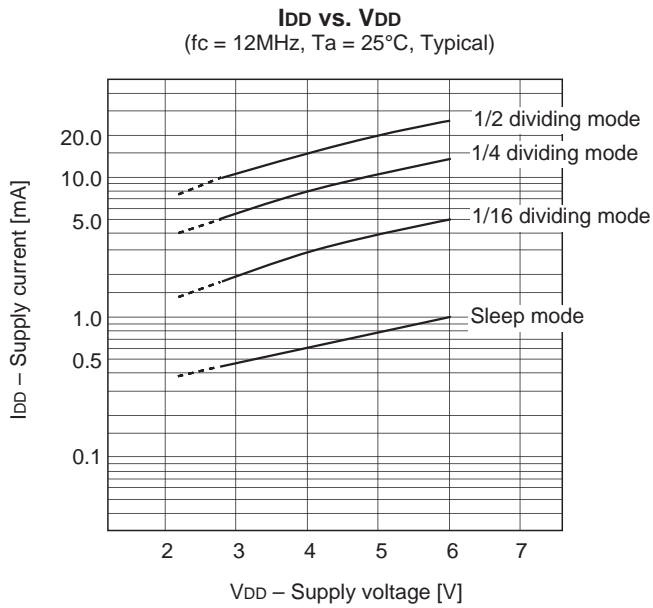
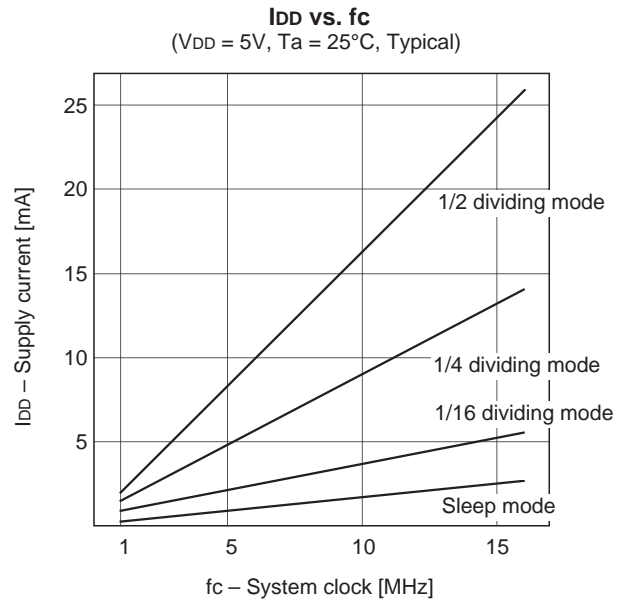
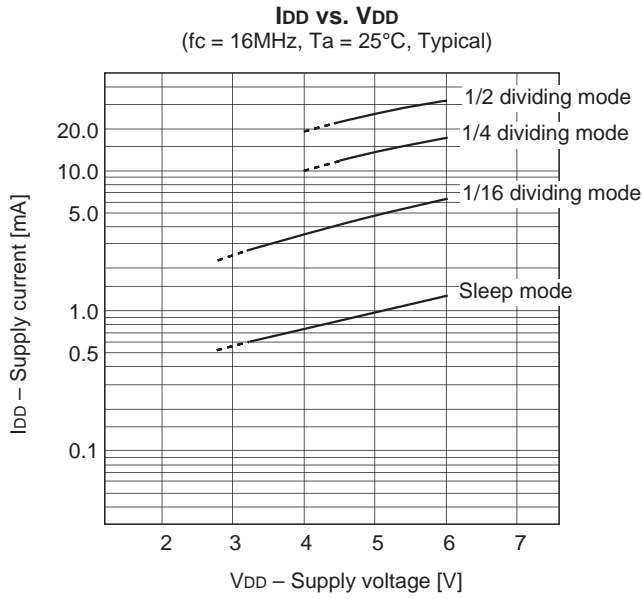
Manufacturer	Model	fc (MHz)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	R <sub>d</sub> (Ω)	Circuit example
RIVER ELETEC CORPORATION	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

Mask Option Table

Item	Content	
	Reset pin pull-up resistor	Non-existent
Power on reset circuit	Non-existent	Existent
General purpose prescaler oscillation circuit	Non-existent	Existent
Input circuit format*1	CMOS schmitt	TTL schmitt

\*1 In PG4/SYNC0/PMI pin and PG5/SYNC1 pin, the input circuit format can be selected every pin.

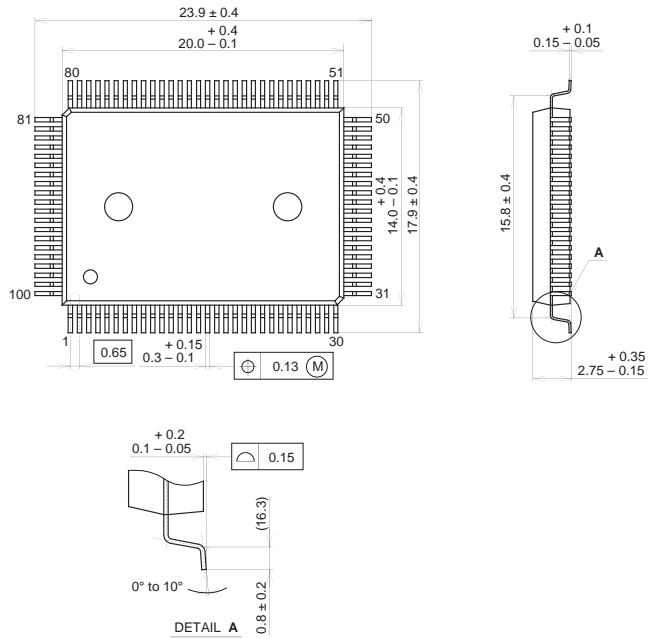
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

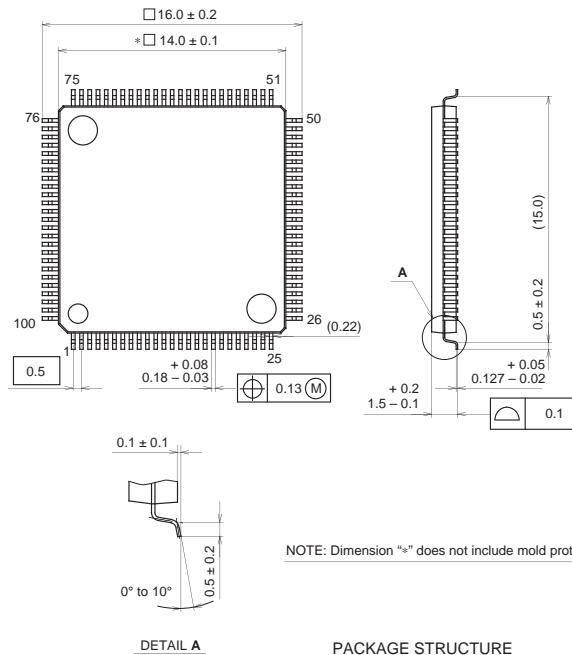


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "±" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g